AMENDMENTS

Amendments to the Specification:

Please replace the paragraph beginning on line 18 of page 13 of the Application with the following amended paragraph.

Referring to the chart of Figure 2, overlay tolerance can be determined for a lot of semiconductor wafers by finding the point that corresponds to the measured critical dimension error in the first patterned layer (CD Error A) and the measured critical dimension error in the second patterned layer (CD Error B). The diagonal line that corresponds to this point is the corresponding overlay tolerance. For example, a CD Error A of 0 and a CD error B of 0 give a point that intersects line ~~20~~ 50 (which indicates an overlay tolerance of 50 nanometers).

Please replace the paragraph beginning on line 13 of page 17 of the Application with the following amended paragraph.

In the embodiment shown in ~~Figure 4~~ FIGS. 4A-4B, critical dimension error measurement of feature 411 (step 302) gives a size measurement indicated by arrow 412. The difference between the size of arrow 412 and the intended size of the feature (arrow 402) is the critical dimension error. Similarly, in step 304, critical dimension error measurements are obtained by measuring the size of feature 413 which is indicated by arrow 414. The difference between the size of arrow 414 and the intended size of the feature (arrow 404) is the critical dimension error.

Please replace the paragraph beginning on line 21 of page 20 of the Application with the following amended paragraph.

In ~~Figure 4~~ FIGS. 4A-4B the overlay error between the first patterned layer and the second patterned layer can be determined by measuring the overlay error between feature 411 in the first patterned layer and feature 413 in the second patterned layer.

For example, in the embodiment shown in ~~Figure 4~~ FIGS. 4A-4B the overlay error is the distance between the centerline A-A of feature 411 and the centerline B-B of feature 413 which is indicated by arrow 415.